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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/381,400	02/03/2000	YOSHINORI MIYAKI	843.37610X00	3904

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/381,400	MIYAKI ET AL.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 09/381400 Attorney's Docket #: 843.7610X00
Filing Date: 2/3/00;

Applicant: Miyaki et al.

Examiner: Alexander Williams

Applicant's Request for Reconsideration, filed 11/25/04, has been acknowledged.

Claims 1 to 21 have been canceled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 22 to 36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kajihara et al. (U.S. Patent # 5,637,913) in view of Yamamoto (Japan Kokai # 63-271939) and further in view of Mori (Japan Patent Application # 3-22465).

In claims 21 and similar claim 29, Kajihara et al. **(figures 1 to 32)** specifically figure 30 show a semiconductor device **30** comprising: a semiconductor chip **2** having a main surface **(top of 2)** and a rear surface (**bottom of 2)** opposite to said main surface, said semiconductor chip having a plurality of semiconductor elements and bonding pads **25** formed on said main surface, and show a insulative film **(topmost layer of 2, but not described)** having openings exposing said bonding pads; a lead frame having a die pad **3** for supporting said semiconductor chip and a plurality of leads **5** each having an inner lead **(inner portion of 5 within 29)** and an outer lead **(outer portion of 5 outside of 29)** that is continuously formed with said inner lead, said plurality of leads arranged to surround said die pad; a plurality of bonding wires **26** electrically connecting said inner leads of said plurality of leads with said plurality of bonding pads respectively; and a resin body **29** sealing said semiconductor chip, said inner leads of said plurality of leads, said die pad and said plurality of bonding wires respectively; wherein a size of said die pad **3** is smaller than a size of said semiconductor chip in a plan view; wherein said semiconductor chip is disposed on said die pad that said rear surface of said semiconductor chip is fixed to said die pad by an adhesive **(inherit, see column 10, lines 45-49 and 55-64)**, wherein parts of said resin body contact with said insulative film of said semiconductor chip and a portion of said rear surface of said semiconductor chip except for an area to which said die pad is fixed. Kajihara et al. show the features of the claimed invention, but fail to detail the semiconductor chip and the layers on top of the semiconductor chip. However, it is understood to one of ordinary skill in the art to understand the cross hatching representing an insulative film on top of the semiconductor chip with exposed bond pad connecting the bonding wires to the pads (see column 10, lines 29-38).

. Nevertheless, Yamamoto is cited for showing a semiconductor device. Specifically, Yamamoto discloses a photosensitive organic film formed on the top of the semiconductor chip with opening exposing the bond pads being connected to the bonding wires, which connects the lead. Yamamoto **(figures 1 to 5)** specifically figure 1d discloses a semiconductor device comprising: a semiconductor chip **5** having a main surface **(top of 5)** and a rear surface (**bottom of 5)** opposite to said main surface, said semiconductor chip having a plurality of semiconductor elements and bonding pads **2** formed on said main surface, and show a organic film **(topmost layer 4)** having openings exposing said bonding pads; a lead frame having a die pad **(middle portion of 6)** for supporting said semiconductor chip and a plurality of leads **6** each having an

inner lead **(inner portion of 6 within 8)** and an outer lead **(outer portion of 6 outside of 6)** that is continuously formed with said inner lead, said plurality of leads arranged to surround said die pad; a plurality of bonding wires **7** electrically connecting said inner leads of said plurality of leads with said plurality of bonding pads respectively; and a resin body **8** sealing said semiconductor chip, said inner leads of said plurality of leads, said die pad and said plurality of bonding wires respectively; wherein said semiconductor chip is disposed on said die pad that said rear surface of said semiconductor chip is fixed to said die pad by an adhesive **(inherit)**, wherein parts of said resin body contact with said organic film of said semiconductor chip and a portion of said rear surface of said semiconductor chip except for an area to which said die pad is fixed, the layer of organic material is made of photosensitive polyimide resins **4** for the purpose of providing a photolithography process that can be finished at one time at the time of opening of the electrode part and having an improved reflow cracking resistance.

Nevertheless, Mori is cited for showing a resin-sealed semiconductor device. Specifically, Mori discloses a polyimide organic film formed on the top and bottom of the semiconductor chip for the purpose of reducing sharply the number of occurrences of resin cracks. Mori discloses that if the main surface of the semiconductor alone is coated, peeling occurs on the interface between the reverse surface of the island part and the sealing resin, the stress is concentrated thereon and consequently the resin crack occurs. If the surface of the island part (rear surface of the semiconductor or die pad) alone is coated, the peeling occurs on the interface between the main surface of the peeling element and the sealing resin, the stress is concentrated thereon, the resin cracks occurs and this a sufficient effect can not be obtained. Therefore, Mori teaches using an organic film on the main surface of the semiconductor and on the die pad connecting the semiconductor chip.

Therefore, it would have been obvious to one of ordinary skill in the art to use Mori's polyimide organic film on both side of the semiconductor chip and Yamamoto's photosensitive polyimide organic film to modify Kajihara et al.'s insulative film for the purpose of providing a photolithography process that can be finished at one time at the time of opening of the electrode part and having an improved reflow cracking resistance.

Claims 22 to 36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Umehara et al. (Japan Patent Application # 9-97806) in view of Mori (Japan Patent Application # 3-22465).

In claims 21 and similar claim 29, Umehara et al**. (figures 1 to 62)** specifically figure 1 show a semiconductor device **83** comprising: a semiconductor chip **10** having a main surface **(top of 10)** and a rear surface (**bottom of 10)** opposite to said main surface, said semiconductor chip having a plurality of semiconductor elements and bonding pads **17** formed on said main surface with the pads exposed to the bond wires and the resin on the main surface; a lead frame having a die pad **81** for supporting said semiconductor chip and a plurality of leads **6,7** each having an inner lead **(inner portion of 7 within 18)** and an outer lead **(outer portion of 6 outside of 16)** that is continuously formed with said inner lead, said plurality of leads arranged to surround said die pad; a plurality of bonding wires **15** electrically connecting said inner leads of said plurality of leads with said plurality of bonding pads respectively; and a resin body **18** sealing said semiconductor chip, said inner leads of said plurality of leads, said die pad and said plurality of bonding wires respectively; wherein a size of said die pad **81** is smaller than a size of said semiconductor chip in a plan view; wherein said semiconductor chip is disposed on said die pad that said rear surface of said semiconductor chip is fixed to said die pad by an adhesive **84**, wherein parts of said resin body contact with said insulative film of said semiconductor chip and a portion of said rear surface of said semiconductor chip except for an area to which said die pad is fixed. Uhehara et al. fail to explicitly show an organic film formed to cover said main surface, said organic film having openings exposing said bond pads detail the semiconductor chip and the layers on top of the semiconductor chip. However, Uhehara et al. does discloses a smaller mount pad which mounts on the rear of a larger chip by an thermoplastic polyimide organic film for the purpose of having a highly reliable package without to reduced package cracks is obtained.

. Nevertheless, Mori is cited for showing a resin-sealed semiconductor device. Specifically, Mori discloses a polyimide organic film formed on the top and bottom of the semiconductor chip for the purpose of reducing sharply the number of occurrences of resin cracks. Mori discloses that if the main surface of the semiconductor alone is coated, peeling occurs on the interface between the reverse surface of the island part and the sealing resin, the stress is concentrated thereon and consequently the resin crack occurs. If the surface of the island part (rear surface of the semiconductor or die

pad) alone is coated, the peeling occurs on the interface between the main surface of the peeling element and the sealing resin, the stress is concentrated thereon, the resin cracks occurs and this a sufficient effect can not be obtained. Therefore, Mori teaches using an organic film on the main surface of the semiconductor and on the die pad connecting the semiconductor chip.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invetion to use Mori's polyimide organic film on both side of the semiconductor chip to modify Umehara et al.'s polyimide film on the die pad with the resin connection to part of the bottom of the semiconductor chip for the purpose of for the purpose of reducing sharply the number of occurrences of resin cracks.

Response

Applicant's arguments filed 12/5/03 have been fully considered, but are not found to be persuasive in view of outstanding grounds of rejections detailed above. Applicant's arguments concerning the organic film disclosed in Kajihara et al. remain outstanding as discussed as an insulative film. Applicant's drawings does not show the combination of the claims organic film and the shorter die pad. They are detailed individually in separate figures. Applicant's Figure 2 shows the details of the die pad with the resin connected to the bottom surface of the semiconductor chip. The Examiner's reference of Kajihara et al..'s figure 30 show this portion of the claim with an insulative film on the main surface of the semiconductor chip. Applicant's figures 3 to 7 detials the organic film on the main surface of the semiconductor chip. There are no figures that show the combination of both in Applicant's drawing. The Examiner reference of Yamamoto et al.'s figure 2 show the details of the organic film with bond pads exposed to wire bonding on the main surface of a semiconductor chip. As detailed above, the claims still remain rejected as in the last office action.

Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT

MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Field of Search	Date
U.S. Class and subclass: 257/676,666,678,684,692,693,700,701,797,787	9/6/01 4/2/02 8/13/02 7/15/03 3/2/04
Other Documentation: foreign patents and literature in 257/676,666,678,684,692,693,700,701,797,787	9/6/01 4/2/02 8/13/02 7/15/03 3/2/04
Electronic data base(s): U.S. Patents EAST	9/6/01 4/2/02 8/13/02 7/15/03

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
3//2/04

Alexander Williams
Primary Examiner